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09/757,798	01/09/2001	Jerry Thomas Bolton JR.	49581-P023US-09906909	7350

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EXAMINER	
TSE, YOUNG TOI	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/757,798	BOLTON, JERRY THOMAS	
	Examiner	Art Unit	
	YOUNG T. TSE	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 10-23* is/are rejected.

7)☒ Claim(s) *7-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 8, line 13 to page 9, line 8, filed July 21, 2004, with respect to reference signs of Figure 12 have been fully considered and are persuasive. The objection of Figure 12 has been withdrawn since the objection is based on the drawings submitted on January 09, 2001, but not the drawings submitted later on April 16, 2002.

2. Applicant's arguments, see page 12, line 22 to page 16, line 2, filed July 21, 2004, with respect to the rejections of claims 1-23 under 35 U.S.C. 102(e) and 103(a) have been fully considered and are persuasive because Applicant submitted a declaration under 37 C.F.R. 1.131 to overcome the filing date of December 12, 2000. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the prior art Figure 5 of the instant application, Shieu (Previously cited by Applicant) and Melanson (Newly cited).

3. Applicant's arguments filed July 21, 2004 (see page 9, lines 18-26; page 10, line 27 to page 11, 14; and page 11, line 27 to page 12, line 2) have been fully considered but they are not persuasive.

With respect to claim 16, see the detailed objection and reasons set forth below.

With respect to claim 10, the examiner disagrees with Applicant's argument that the multi-stages shown in Figures 6 and 7 may consider as the multi-stage delta-sigma modulator in the first delta-sigma modulator. Figure 6 shows a second-order delta-

sigma modulator while Figure 7 shows a third-order delta-sigma modulator. For the same reasons discussed in the previous Office Action of Figure 8, block element 61 of Figure 6 (the same elements shown in Figure 7) is the first delta-sigma modulator, however, block 62 of Figure 6 and block 73 of Figure 7 are the at least one subsequent delta-sigma modulator as recited in claim 1.

With respect to claim 20, clearly, the means for providing the modulated output signal to an output of the multi-order delta-signal modulator is not shown in Figure 8 because the output 6001 is the output of the summing circuit 600 which is also the output of the multi-order delta-signal modulator.

Drawings

4. The drawings were received on July 21, 2004. These drawings (replacement sheets 3/8 to 8/8) are acceptable.

Specification

5. The disclosure is objected to because of the following informalities: on page 8, line 2, "3-1=2" should be "4-1=3". Appropriate correction is required.

Claim Objections

6. Claims 1-14 and 16 are objected to because of the following informalities:

In claim 1 (line 7) and claim 4 (line 3), the phrase "said set" should be "said set of differentiators".

In claim 12, line 1, "invention" should be "modulator".

In claim 16, line 3, "a revised input" should be "an intermediate input signal" since the specification lacks support of "a revised input" and to avoid the lacking of antecedent basis of "said integrated input signal" recited in line and 7 of the claim, line 4, "said integrated input" should be "said integrated input signal" to avoid the lacking of antecedent basis of "said quantized signal", and line 5, "said revised input" should be "said intermediate input signal". Wherein dependent claims 2-3, 5-11 and 13-14 are depended upon claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 20-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The configuration of claim 20 does not correspond to the disclosure of the drawings. For example, claim 20 recites means for providing said modulated output signal to an output of said multi-order delta-sigma modulator, however, no additional circuitry is shown other than the summing circuit 600 of Figure 8 for providing said

modulated output signal to an output of said multi-order delta-sigma modulator.

Wherein the dependent claims 21-23 are depended upon claim 20.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 12, lines 2-3, the phrase "said input signal" lacks clear antecedent basis.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

12. Claims 1-6, 11 and 13-15 are rejected under 35 U.S.C. 102(a) as being anticipated by the prior art Figure 5 of the instant application.

The prior art Figure 5 of the instant application discloses a MASH fourth-order or multi-stage delta-sigma modulator 5.

The fourth-order or multi-stage delta-sigma modulator 5 comprises a first delta-sigma stage 510, a second delta-sigma stage 520, a third delta-sigma stage, a fourth delta-sigma stage 540, and a summation circuit 500 for summing the modulated signal of the four delta-sigma modulators to produce a multi-order modulated signal. Each

delta-sigma stage includes an adder 50, a quantizer 51, a feedback circuit including a summation circuit 52 and a delay circuit 53. The second to fourth delta-sigma stages further include differentiators 54. Also see page 7, line 22 to page 11, line 29 of the specification.

With respect to claims 1 and 15, the first delta-sigma stage 510 corresponds to the first delta-sigma modulator of a first stage having a first reference signal (the output of the quantizer 51); the second to fourth delta-sigma stages correspond to the at least one subsequence delta-sigma modulator of at least one subsequence stage cascade from the first stage having a reference signal (the output of the quantizers 51) variable in relation to the first reference signal; and the differentiators 54 in each of the second to fourth delta-sigma stages correspond to the set of differentiators coupled to the output of the quantizers 51. Notice the output of the quantizer 51 in each of the delta-sigma stages has different reference signal.

With respect to claim 2, the summation circuit 500 for summing the output of each of the delta-sigma stages.

With respect to claim 3, the input signal N(z) of the fourth-order or multi-stage delta-sigma modulator 5 is digital signal.

With respect to claim 4, the second delta-sigma stage 520 has one differentiator 54, the third delta-sigma stage has two differentiators 54, and the fourth delta-sigma stage 540 has three differentiators 54.

With respect to claim 5, the fourth-order or multi-stage delta-sigma modulator 5 comprises three subsequence or second to fourth delta-sigma modulators.

With respect to claim 6, the reference signal in each of the delta-sigma modulators is different from each other as mentioned in claims 1 and 15 above.

With respect to claim 11, the second to fourth delta-sigma modulators are multi-stage delta-sigma modulators.

With respect to claims 13 and 14, delta-sigma modulators are fabricated on a single integrated circuit substrate are well known in the delta-sigma modulator communication art as mentioned on page 11, lines 18-19 of the instant application.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art Figure 5 of the instant application as applied to claim 1 and claim 15 mentioned above in view of Melanson (Newly cited).

With respect to claim 12 and claim 19, the prior art Figure 5 of the instant application fails to show or suggest that an interpolation circuit is used prior the fourth-order or multi-stage delta-sigma modulator 5 for increasing a sampling rate of the input signal N(z).

Melanson (US Patent No. 6,373,417 B1) discloses an oversampling digital to analog converter in Figure 1 having a delta-sigma converter or modulator 114 and a pulse width modulator 116 as a demodulator 112; and interpolation blocks 104, 106, 108 and 110 raise the data rate of an input signal 102 to the input of the delta-sigma converter or modulator 114. See column 1, lines 24-27.

Therefore, it would have been obvious to one of ordinary skill in the art to insert an interpolation circuit prior to the fourth-order or multi-stage delta-sigma modulator 5 of Figure 5 of the instant application as taught by Melanson for the purpose of increasing a data or sampling rate of the input signal N(z) of the fourth-order or multi-stage delta-sigma modulator 5.

15. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art Figure 5 of the instant application as applied to claim 15 discussed above in view of Shieu (Previously cited by Applicant).

With respect to claims 16-19, the prior art Figure 5 of the instant application fails to show or suggest that an integrator is provided between the summation circuit 50 and the qnantizer 51 in each of the stage of the delta-sigma modulators.

Shieu (U.S. Patent No. 5,191,332) discloses an oversaming converter circuit in Figure 2 having a third-order stage delta-signal modulator, wherein each stage of the delta-signal modulators comprises the similar block elements as shown in the prior art Figure 5 of the instant application. Further, each stage also comprises an integrator 23, 25, or 29 connected between a summation circuit 22, 27, or 28 and a comparator or quantizer 24, 26, or 201, and the summation circuit 207 or 208 for subtracting the output

of the quantizer 24 or 26 from the output of the integrator 23 or 25 as recited in the claimed subject matter of claims 16-19.

Therefore, it would have been obvious to one of ordinary skill in the art to insert an integrator in each of the stage of the delta-sigma modulators in the prior art Figure 5 of the instant application between the summation circuit 50 and the qnantizer 51 as taught by Shieu in order to produce a quantization error signal by the summation circuit 52 between the outputs of the inserted integrator and the quantizer 51 in each of the stage of the delta-sigma modulators.

Allowable Subject Matter

16. Claims 7-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. Claims 20-23 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, first paragraph, set forth in this Office action.

18. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to show or suggest that the reference signal in each of the subsequence second to fourth stages of the delta-signal modulators has substantially equal reference signals or is selectively variable in relation to the first reference signal of the first stage of the delta-sigma modulator.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

References Jelonneck et al. and Cole are made of record as describing a related multi-stage or multi-order delta-signal modulator having a plurality of stages.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday and Wednesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2637